WHAT IS CLAIMED IS

1. A low power RF receiver including an antenna for receiving radio-frequency signals originating from satellites, a reception and shaping stage for the radio-frequency signals provided by the antenna, a correlation stage formed of several channels which each include a correlator, said correlation stage receiving intermediate signals shaped by the reception stage, a microprocessor connected to the correlation stage and intended to calculate X, Y and Z position, velocity and time data as a function of data extracted, after correlation, from the radio-frequency signals transmitted by the satellites, wherein, in each channel, a controller, including a digital signal processing algorithm, is associated with the correlator to allow all the synchronisation tasks to be performed autonomously for acquiring and tracking a satellite when the channel is set in operation, and wherein at least a set of data input and output registers is placed at the interface between the correlation stage and the microprocessor in order to receive data transmitted by the microprocessor to the correlation stage and data supplied from the correlation stage, said data passing through the set of registers being formed of signals of a frequency lower than or equal to the frequency of the message signals, so that the microprocessor can perform the tasks of calculating the position, velocity and time without any intervention as regards the synchronisation and correlation tasks.

2. A RF receiver according to claim 1, wherein the intermediate signals provided to the correlation stage are complex signals which have been sampled and quantified in the reception and shaping stage, these complex signals being formed of a 1-bit in-phase signal component and a 1-bit quarter-phase signal component.

3. A RF receiver according to claim 1, wherein the controller acts on control loops of the C/A code phase and the carrier frequency in a bit-parallel architecture.

4. A RF receiver according to claim 1, wherein each correlator is formed of a first multiplier stage for multiplying the intermediate signals with on the one hand the cosine minus i times the sine of the replica of the carrier frequency generated digitally in the correlation stage and with on the other hand the minus sine minus i times the cosine of this carrier frequency replica to provide at output a first in-phase signal and a second quarter-phase signal, of a second multiplier stage for correlating the first signal with on the one hand a late replica of the satellite C/A code signal digitally generated in the correlation stage and with on the other hand an early replica of the satellite C/A code signal and to correlate the second signal with on the one hand a late replica of the satellite C/A code signal and on the other hand an early replica of the satellite C/A

code signal, the four signals leaving the second multiplier stage being each passed into a respective integrator counter to provide four in-phase and quarter-phase code signals each distributed over at least 8 bits in a C/A code phase correction loop, and the sum of the two in-phase code signals and the sum of the two quarter-phase code signals providing two carrier signals each distributed over at least 8 bits in a carrier frequency correction loop.

5. A RF receiver according to claim 4, wherein the early signals have a phase offset of a half chip with respect to the late signals.

6. A RF receiver according to claim 4, wherein the code correction loop includes in succession a code loop discriminator, a code loop filter, a 28-bit NCO oscillator, a C/A code generator connected to a 2-bit register supplying the early and late replicas to the second multiplier stage.

7. A RF receiver according to claim 4, wherein the carrier frequency correction loop includes in succession a carrier loop discriminator, a carrier loop filter, a 24-bit NCO oscillator and two units for providing to the first multiplier stage of the cosine and the sinus of the replica of the carrier frequency corrected by the NCO oscillator.

8. A RF receiver according to claim 1, wherein it includes 12 channels with a correlator and a controller for each of them.

9. A RF receiver according to claim 1, wherein a first part of the correlator and the controller of each channel is clocked by a first clock signal provided by a quartz oscillator housed in the reception and shaping stage, and wherein a second part of the correlator and the controller is clocked by a second clock signal, the frequency of the first clock signal being 16 times greater than the frequency of the second clock signal.

10. A RF receiver according to claim 1, wherein a set of registers is provided for each channel.

11. A RF receiver according to one of claims 1 and 10, wherein the correlation stage, the set or sets of registers and the microprocessor are made in a single semiconductor substrate.

12. A watch including a RF receiver according to claim 1, wherein the RF receiver is housed in the case of the watch and is powered by an energy accumulator or a battery also used for powering the electronic components for the horological functions.